AMENDMENTS TO THE SPECIFICATION

Please replace the six paragraphs beginning on page 1, line 23 and continuing onto page 3 with the following amended paragraphs:

If a bank is in a state where the bank has been already pre-charged and closed, the same bank, when being accessed next time, can be accessed at a constant speed regardless of its address. However, ~~in a case~~ where a bank has not been pre-charged but has been opened, if a same page as its bank has previously opened is to be accessed, since opening of the page is not required, the bank can be accessed speedily when compared with ~~the case where~~ the bank that has been closed. However, when accessing a page that is different from a page whose bank has been opened ~~is to be accessed, since the page to which access is obtained has to be opened after the bank has been pre-charged~~, the bank ~~can~~ will be accessed at a slower speed when compared ~~with the case where~~to the closed bank ~~has been closed~~ because the accessed page must be opened after the bank has been pre-charged.

~~Access to a same~~Finding data on a given page is called a "hit" and ~~access to a different page~~failure to find data on a given page is called a "miss".

A memory control device employing a conventional open page policy, wherein access efficiency is improved by changing the time at which a bank is closed according to a number of hits to the bank, is disclosed in ~~which access efficiency is improved by changing the timing with which a bank is closed according to the number of hits to a bank~~ (Japanese Patent Application Laid-open No. 2001 -166985).

Both the closed page policy and open page policy have problems. ~~That is, the~~ The closed page policy heightens access performance when ~~a~~ the probability of a hit is low, while the open page policy heightens ~~the~~ access performance when a probability of the

hit is high. However, neither ~~the closed page~~ policy ~~nor the open page policy can make~~will enable a system to ~~the access performance~~ reach its theoretical limit for access performance.

~~The conventional memory control device has a problem. That is,~~Further, in ~~the~~ a memory control device employing ~~the~~ an open page policy, wherein the time at which ~~in which timing with which~~ a bank is closed is changed according to the number of hits to a the bank, ~~since the bank is always kept opened after access has been obtained, if a miss is~~misses are found continuously in a short interval, the access efficiency of the device will~~is~~ not improved because the bank is always kept open after each access attempt.

Moreover, the conventional memory control device has another problem. That is, when the shortest ~~timing~~ time with which a bank is closed is set to be shorter than an interval for access to a memory, since the operation becomes the same as ~~in the case~~that of the closed page policy, if many hits are found, there is no improvement of access efficiency.

Please replace the paragraph beginning on page 3, line 8 with the following amended paragraph:

In view of the above, it is an object of the present invention to provide a memory access control device capable of enhancing memory access efficiency by predicting whether or not a hit is found in a subsequent access.

Please replace the two paragraphs beginning on page 3, line 18 with the following amended paragraphs:

a hit predicting unit to predict whether or not next access to each bank in memory ~~becomes~~ is access to a same page;

wherein the memory control unit, when a hit predicting unit predicts that a next access to the bank will be directed to a same page, that is, that a hit is found, terminates its routine without closing a bank being presently accessed at the time of completion of present access operations and, when the hit predicting unit predicts that next access to the bank ~~becomes~~ is access to a different page, that is, that a miss is found, closes the bank being presently accessed at the time of completion of present access operations and terminates its routine.

Please replace the paragraph beginning on page 11, line 16 with the following amended paragraph:

A memory master 1 outputs a request signal requesting a right to use memory, an address signal, a read / write signal showing types of accesses, a word length signal indicating the number of words to be accessed, a write data signal, and a data mask signal to the memory control section 3. The memory master 1 also receives an acknowledge signal and a read data signal indicating acquisition of a memory ~~right~~ from the memory control section 3.

Please replace the three paragraphs beginning on page 12, line 3 with the following amended paragraphs:

A hit predicting section 4 outputs a plurality of hit prediction results to the memory control section 3. The number of hit prediction results is the same as the total number of banks in all memories being connected. For example, if two memories 5 and 6, each being made up of four banks, are connected, since an entire system has eight banks, the prediction number obtained as the hit prediction results becomes eight.

The memory master 1, when access to memory is required, asserts or initiates a request signal and, at the same time, outputs an address signal, a read / write signal, a word length signal, a write data signal, and a data mask signal in a predefined format.

The memory control section 3, when the request signal fed from the memory master 1 is asserted, receives the address signal, the read / write signal, and the word length signal, and produces a control signal for memory if the read / write signal indicates "write access" to get access for writing and, if the read / write signal indicates "read access", to get access for reading.

Please replace the paragraph beginning on page 13, line 10 with the following amended paragraph:

Moreover, though the memory control section 3 determines whether or not to close a bank being presently accessed ~~is closed~~ by making a reference to the bank storing the last data, if the next data is stored in a bank different from the bank being presently accessed, the memory control section 3 determines whether or not to close the bank being presently accessed ~~is closed~~ by making a reference to the hit prediction result fed from the hit predicting section 4.

Please replace the paragraph beginning on page 13, line 24 with the following amended paragraph:

The memory control section 3~~,~~ stores a page address of each bank that was accessed last. ~~If the page address indicates, at~~At a time of starting a next access, if the page address indicates the same page as that having been accessed the previous time, the memory control section 3 asserts a hit signal corresponding to a bank.

Please replace the two paragraphs beginning on page 14, line 1 with the following amended paragraphs:

Moreover, ~~the memory control section 3,~~ at a time of starting an access, if the page address indicates a page different from the page having been accessed the previous time, the memory control section 3 asserts a miss signal corresponding to a bank.

The time when access is started includes not only a time when first access is started after a request signal fed from the memory master 1 has been asserted but also a time when the next access is started upon completion of storing of ~~if~~ each of data being presently accessed and data to be accessed next ~~is stored~~ in each of different banks before access to a length of words indicated by a word length signal ~~is completed~~.

Please replace the two paragraphs beginning on page 15, line 7 with the following amended paragraphs:

Moreover, after this, if a miss signal is asserted, the number of times of asserting hit signals is four in the most recent eight times asserting operations, and if ~~not~~ instead of a miss signal ~~but~~ a hit signal is asserted, the number of times of asserting hit signals is five and no change occurs. Moreover, "n" is determined at the time of system design and "m" is made variable depending on setting.

Next, operations of the hit predicting section 4 corresponding to another embodiment shown in Figure 2 will be described. ~~The hit predicting section 4,~~ ~~every~~Every time a hit signal or a miss signal fed from the memory control section 3 is asserted, the hit predicting section 4 stores the result of the assertion, corresponding to the number of times of asserting the signals in recent "j" ("j" denotes a natural number) asserting times for each bank.

Please replace the two paragraphs beginning on page 16, line 3 with the following amended paragraphs:

Moreover, after this, if a miss signal is asserted, the number of times of asserting a hit signal is three in the most recent four times asserting operations, so that a hit prediction result of the bank indicates that a miss is found. If ~~not~~ instead of a miss signal ~~but~~ a hit signal is asserted, a hit prediction result of the bank indicates ~~that~~ a hit ~~remains to be~~is found. Moreover, "j" is made variable depending on setting.

Next, operations of the hit predicting section 4 corresponding to yet another embodiment shown in Figure 2 will be described. ~~The hit predicting section 4, every~~Every time a hit signal or a miss signal fed from the memory control section 3 is asserted, the hit predicting section 4 stores the result of the assertion, corresponding to the number of times of asserting the signals in recent "k" ("k" denotes a natural number) times asserting operations for each bank.

Please replace the two paragraphs beginning on page 16, line 28 with the following amended paragraphs:

Moreover, after this, if a hit signal is asserted, the number of times of asserting a miss signal is three in the most recent four times asserting operations, a hit prediction result of the bank indicates that a hit is found. If ~~not~~ instead of a hit signal ~~but~~ a miss signal is asserted, a hit prediction result of the bank indicates that a miss ~~remains to be~~is found. Moreover, "k" is made variable depending on setting.

Next, operations of the hit predicting section 4 corresponding to still another embodiment shown in Figure 2 will be described. ~~The hit predicting section 4, every~~Every time a hit signal or a miss signal fed from the memory control section 3 is asserted, the hit predicting section 4 stores the result of the assertion, corresponding to the number of times of asserting the signals in recent "n" ("n" denotes a natural number) times asserting operations for each bank.

Please replace the paragraph beginning on page 17, line 26 with the following amended paragraph:

The hit predicting section 4 judges whether the number of times of asserting a hit signal for each bank is "m" times or more ($m \leqq n$: "m" and "n" each is a natural number) in recent "n" times asserting operations and, if the number of times of asserting a hit signal is "m" times or more, outputs information indicating that a hit is found as a hit prediction result and, if not, outputs~~, if NOT,~~ information indicating that a miss is found.

Please replace the three paragraphs beginning on page 19, line 15 with the following amended paragraphs:

The memory control section 3, when getting access to the last data, determines whether or not a to close bank being presently accessed ~~is closed~~ depending on a hit prediction result fed from the hit predicting section 4. At this point, ~~the memory control section 3,~~ if the memory master 1 outputs a next address confirming signal and when a bank and a page indicated by its next address signal are matched to the bank and the page being presently accessed, the memory control section 4 terminates its routine without closing ~~a~~ the bank being presently accessed, regardless of a hit prediction result fed from the hit predicting section 4.

On the other hand, ~~the memory control section 3,~~ while the memory master 1 outputs an address confirming signal and if only the bank, ~~out~~ of the bank and the page indicated by its address signal, is matched to the bank, ~~out~~ of the bank and the page being presently accessed, and if the page, ~~out~~ of the bank and the page indicated by its address signal, is not matched to the page, ~~out~~ of the bank and the page being presently accessed,

the memory control section 3 closes the bank being presently accessed and terminates its routine, regardless of a hit prediction result fed from the hit predicting section 4.

For example, ~~let it be assumed~~assume that the memory master 1 is now getting access to a bank and a page and its last address is a bank 0 and a page 0. If the memory master 1 has asserted a next address confirming signal and if both a bank and a page indicated by a next address signal fed from the memory master 1 are 0, the memory control section 3 terminates its routine without closing the bank 0 at the time when the memory master 1 completes its access, regardless of a hit prediction result fed from the hit predicting section 4.

Please replace the paragraph beginning on page 20, line 20 with the following amended paragraph:

If the bank 0 ~~has~~ had been closed at the time when the memory master 1 completes its access, access to memory ~~has~~ would have to be started after having made the bank 0 active and time is spent before the next access to memory is started.

Please replace the paragraph beginning on page 21, line 14 with the following amended paragraph:

Each of the memory masters 1-1 to 1-4 outputs a request signal for requesting a right ~~of using~~to use memory, an address signal, a read / write signal showing a type of access, a word length signal showing the number of words to be accessed, a write data signal, and a data mask signal to an arbiter section 2 and receives an acknowledge signal showing acquisition of ~~using~~ memory for use and read data signal from the arbiter section 2.

Please replace the paragraph beginning on page 21, line 2 with the following amended paragraph:

Though the memory master 1 next gets access to the bank 0 in memory, since the bank 0 ~~has~~ had been closed~~,~~ after previous access by the memory master 1 ~~has~~ had been completed, the bank 0 is immediately made active and, after the bank 0 has been made active, memory can be accessed.

Please replace the two paragraphs beginning on page 23, line 4 with the following amended paragraphs:

As a method for selecting one memory master from two or more memory masters, there is a method by which one memory master is selected according to a predetermined priority order, a method by which one memory master in priority order most ~~far~~ removed or farthest from the time when last access is obtained is selected according to a round-robin method, and the like.

The memory control section 3, when a request signal fed from the arbiter section 2 is asserted, receives an address signal, a read / write signal, and a word length signal, and produces a control signal for memory to get write access, if a read / write signal indicates ~~writeaccess~~write-access, and, to get read access if the read / write signal indicates read-access.

Please replace the two paragraphs beginning on page 25, line 20 with the following amended paragraphs:

The memory control section 3, when last data is accessed, determines whether or not to close a bank ~~is closed or not~~ by making reference to a hit prediction result fed from the hit predicting section 4. At this point, if there is one or more of the memory masters that are outputting a next address confirming signal and if there is a memory master in which both the bank and the page indicated by its next address signal are matched to both the bank and the page being accessed presently, the memory control section 3 terminates

its routine without closing the bank being presently accessed, regardless of a hit prediction result fed from the hit predicting section 4. Also, the arbiter section 2, when selecting a memory master that accesses memory next, selects a memory master in which both the bank and the page indicated by the next address signal are matched to both the bank and the page being accessed presently.

On the other hand, ~~the memory control section 3,~~ if there is one or more memory masters that are outputting a next address confirming signal, and if there is a memory master in which only the bank, ~~out~~ of the bank and the page indicated by its next address signal, is matched only to the bank, and the page, ~~out~~ of the bank and the page indicated by its next address signal, is not matched to the page being accessed presently, the memory control section 3 closes the bank being accessed and terminates the memory control section's routine, regardless of a hit prediction result fed from the hit predicting section 4.

Please replace the paragraph beginning on page 27, line 23 with the following amended paragraph:

~~Even if~~If either a memory master 1-2 or a memory master 1-3 subsequent to the memory master 1-1 is selected, access is obtained to the bank 0 in memory. However, since the bank 0 is closed, after the memory master 1-1 has accessed the bank, the bank 0 can be made active and, after the bank 0 has been made active, memory can be accessed.

Please replace the paragraph beginning on page 28, line 10 with the following amended paragraph:

Moreover, the hit predicting section 4 has blocks, each of which has the configurations shown in Fig. 7, ~~being~~ equal in number to the banks, which are not shown. In addition to this, the hit predicting section 4 also has a section (not shown) to receive an

instruction for setting of "j-1", "k-1", and "m" (instruction for setting "j", "k", and "m") and to hold these set values.

Please replace the paragraph beginning on page 31, line 3 with the following amended paragraph:

When a hit is predicted, no pre-charge is performed at the time of completion of access. If a miss occurs in the next access, after pre-charge command (#RAS and #WE are made LOW at the same time) has been issued, issuance of the LOW active command (#RAS is made LOW) following switching of A0 to A9 to LOW address is required, so that the next access is obtained later.